REMARKS/ARGUMENTS

Claims 1-19 were previously pending in the application. Claim 13 is canceled; claims 4-5, 8-9, and 17-18 are amended; and new claims 20-21 are added herein. Assuming the entry of this amendment, claims 1-12 and 14-21 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

Support for the amendments to claims 4, 8, and 17 is found in original claim 15. Support for the amendments to claims 5, 9, and 18 is found in original claim 16. Support for new claims 20-21 is found in Fig. 1.

In paragraph 1 of the office action, the Examiner rejected claims 1-10 under 35 U.S.C. 102(b) as being anticipated by Davenport. In paragraph 2, the Examiner rejected claims 11-14 and 17-19 under 35 U.S.C. 103(a) as being unpatentable over Davenport. In paragraph 3, the Examiner objected to claims 15-16 as being dependent upon a rejected base claim, but indicated that those claims would be allowable if rewritten in independent form. For the following reasons, the Applicant submits that all of the now-pending claims are allowable over the cited references.

The Examiner cited Fig. 2 of Davenport in rejecting certain claims in the present application. In doing so, the Examiner suggested that certain elements in Fig. 2 of Davenport are analogous to elements in Fig. 1 of the present application. In particular, the Examiner suggested that:

- Davenport's FET 104 is similar to the present application's transistor M0;
- Davenport's FET 140 is similar to the present application's transistor M1;
- Davenport's FET 102 is similar to the present application's transistor M2; and
- Davenport's FET 124 is similar to the present application's transistor M4.

The Applicant submits, however, that these analogies are not all correct and that the circuitry of the present application's Fig. 1 differs from the circuitry of Davenport's Fig. 2 in at least one significant way. In the present application's Fig. 1, the drain of transistor M2 is connected to the source of transistor M4. In Davenport's Fig. 2, however, the drain of FET 102 is not connected to either channel node (i.e., source or drain) of FET 124. Rather, in Davenport's Fig. 2, the drain of FET 124 is connected to the gate of FET 102. As such, FET 124 does not sense the drain current of FET 102. Moreover, since FET 124 does not sense the drain current of FET 102, the current mirror formed by FETs 104 and 140 does not multiply a sensed drain current of FET 102 for application to the output of FET 102.

Claims 1 and 6

According to claim 1, an input signal is applied to a source follower, the drain current of the source follower is sensed and multiplied, and the multiplied sensed drain current is applied to the output of the source follower. As described above, Davenport does not teach or even suggest circuitry in which the drain current of a source follower is sensed, multiplied, and applied to the output of the source follower.

As such, the Applicant submits that claim 1 is allowable over Davenport. For similar reasons, the Applicant submits that claim 6 is allowable over Davenport. Since claims 2-5 and 7-10 depend variously from claims 1 and 6, it is further submitted that those claims are also allowable over Davenport.

Claims 2 and 7

According to claims 2 and 7, a folded cascode device senses the drain current of the source follower. There is no teaching or even suggestion in Davenport, the FET 124 is a folded cascode device. The Applicant submits that this provides additional reasons for the allowability of claims 2 and 7 over Davenport.

Claims 4 and 8

According to currently amended claim 4, the source follower and the current mirror are both implemented using a first type of device, and the drain current is sensed using a device of a second type different from the first type. The Applicant submits that this provides additional reasons for the allowability of claim 4 (and also claim 8) over Davenport.

Claim 11

According to claim 11, both transistor M2 and transistor M4 are connected at their first channel nodes to the second channel node of transistor M3. As such, the first channel node of M2 is connected to first channel node of M4. However, as described earlier, in Davenport's Fig. 2, no channel node of FET 102 is connected to a channel node of FET 124. Rather, the drain of FET 124 is connected to the gate of FET 102, and the drain of FET 102 is connected to V_{DD}.

As such, the Applicant submits that claim 11 is allowable over Davenport. Since claims 12-19 depend variously from claim 11, it is further submitted that those claims are also allowable over Davenport.

Claim 14

According to claim 14, transistor M4 senses the drain current of transistor M2, and the current mirror multiplies the sensed drain current and applies the multiplied sensed drain current to the output VOUT (i.e., the output of the source follower). As described earlier, Davenport does not teach or even suggest circuitry in which the drain current of a source follower is sensed, multiplied, and applied to the output of the source follower. The Applicant submits that this provides additional reasons for the allowability of claim 14 over Davenport.

Claim 17

According to currently amended claim 17, the source follower and the current mirror are both implemented using a first type of device, and the transistor M4 is of a second type different from the first type. The Applicant submits that this provides additional reasons for the allowability of claim 4 (and also claim 8) over Davenport.

New Claims 20-21

According to new claim 20, a current generated by a current source is applied to both the source follower and a device used to sense the drain current of the source follower. Davenport does not teach or even suggest applying the current from a current source to both FET 102 and FET 124. Moreover, the Applicant submits that, if the circuitry taught in Davenport were modified to apply the current from a current source to both FET 102 and FET 124, the resulting circuitry would not be able to provide the differential level shifting buffer function of Davenport's invention. As such, the modification needed to

achieve the present invention would destroy the functionality of the prior-art teachings. In that case, under U.S. patent law, such modification would not be obvious. See, e.g., In re Gordon, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). The Applicant submits therefore that this provides additional reasons for the allowability of claim 20 (and also claim 21) over Davenport.

In view of the foregoing, the Applicant submits therefore that the rejections of claims under Sections 102(b) and 103(a) have been overcome.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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